described in the abovecited U.S. Patent Application # 09/611,623 that it is often advisable to employ an additional solder mask 702 or polyimide layer with an opening 704 for each solder ball. This technique keeps the flip-chip bump in a defined area and shape during bump formation and subsequent attachment to an external package or board.--

A4 cont.

On page 18, in the first paragraph, please delete the paragraph and insert the following:

Outermost metal layer 165 is equally well suited for wedge bonding, involving ribbons (800 in Figure 8).

A5

In the Claims:

Please amend the claims as follows:

4. (amended) A semiconductor device wherein electrical parasitics are minimized by individualized power distributors deposited over active integrated circuit components, comprising:

a semiconductor chip having first and second surfaces;

A6

an integrated circuit fabricated on said first chip surface, said circuit having active components, contact pads, at least one metal layer, and being protected by a mechanically strong, electrically insulating overcoat having a plurality of metal-filled vias to contact said at least one metal layer;

electrically conductive films deposited on said overcoat and patterned into a network of lines substantially vertically over said active components, said films in contact with said vias and having an outermost film of non-corrodible, metallurgically attachable metal;

said network patterned to distribute power current while minimizing parasitic electrical losses between said network and said active components;

said network further patterned to minimize silicon real estate consumed by power interconnections between said active components;

A6 cont.

a leadframe having a chip mount pad, a first plurality of segments providing electrical signals, and a second plurality of segments providing electrical power and ground;

said second chip surface attached to said chip mount pad;

electrical conductors connecting said contact pads with said first plurality of segments; and

electrical conductors connecting said network lines with said second plurality of segments.

✓6. (cancelled)

✓10. (cancelled)

✓12. (cancelled)

A7

15. (amended) The device according to Claim 4 wherein said electrical conductors are selected from a group comprising wire ball and stitch bonding, ribbon bonding, and soldering.

✓24-28 (cancelled)

Please add the following new claims:

A8

29. (new) An integrated circuit chip mounted on a leadframe, said leadframe having a plurality of segments, comprising:

a network of power distribution lines deposited on the surface of said chip over active components of said circuit;

said lines comprising a stack including a stress-absorbing metal film;

said lines connected vertically to said components by metal-filled vias, and also to said segments by conductors; and

the majority of said lines patterned as straight lines between said vias and said conductors.

30. (new) The device of Claim 29, wherein said stack including a stress-absorbing metal film comprises an outermost metallurgically attachable film.

31. (new) The device of Claim 29, wherein said stack including a stress-absorbing metal film comprises a layer of seed metal, a stress-absorbing metal layer on said seed metal layer, and an outermost metallurgically attachable metal layer.

A8 cont.

32. (new) The device of Claim 31, wherein said stress-absorbing metal layer comprises at least one layer selected from a group consisting of copper, nickel, aluminum, and alloys thereof.

33. (new) The device of Claim 31, wherein said seed metal is selected from a group consisting of tungsten, titanium, titanium nitride, molybdenum, chromium, and alloys thereof.

34. (new) The device according to Claim 31, wherein said outermost metal layer is selected from a group consisting of pure or alloyed aluminum, gold, palladium, silver and platinum.